SEMICONDUCTOR DEVICE AND METHOD OF PROVIDING REGIONS OF LOW SUBSTRATE CAPACITANCE

Background of the Invention

[0001] The present invention relates in general to semiconductor devices and, more particularly, to integrated circuits having components formed on a low capacitance region of a semiconductor die.

[0002] Semiconductor technology continues to scale transistors to have smaller dimensions in order to provide increased functionality and a higher frequency capability. For example, wireless communication devices often use integrated circuits that include high-density digital signal processing functions on the same die as analog circuits operating at frequencies in excess of five gigahertz.

[0003] However, some integrated circuit components, such as passive devices, are not readily scalable. These devices have relatively high parasitic substrate capacitances, which often limits the overall frequency capability of an integrated circuit. For example, inductors are not easily reduced in size without reducing their quality factor or inductance to an unacceptable level, and bonding pads are not scalable because of the need to attach wire bonds to the bonding pads.

[0004] A variety of techniques have been tried to reduce the parasitic capacitances of passive integrated circuit components. One such technique is to form the components over a low permittivity material. However, current low permittivity materials are limited to film thicknesses that are too thin to produce a substantial reduction in parasitic capacitance. Another approach is to form the components over a thick dielectric film in which are formed air gaps or voids that reduce the overall permittivity of the dielectric

film. Previously, voids were formed using thermally grown dielectric films to form the trench, and deposited films to seal them. However, voids made with such films introduce substantial stress in a semiconductor substrate, which degrades the performance and reliability of the integrated circuit. Also, these voids are not optimized for reducing capacitance due to the relatively high dielectric constant of the films used to form them. Furthermore, the voids are filled with these films during the sealing process producing a void with increased dielectric constant. Other schemes reduce the stress by producing fewer voids or voids with only a limited volume, which has a correspondingly limited effect on parasitic capacitance. Moreover, in order to avoid contaminating the transistors or reducing the die yield or reliability, complex and costly schemes are required to enable the integration of the low permittivity structures with active devices such as transistors.

[0005] Hence, there is a need for a low capacitance structure and method of making an integrated circuit that maintains a low cost while reducing die stress and avoiding the introduction of contaminants into the integrated circuit.

Brief Description of the Drawings

[0006] FIG. 1 is a cross-sectional view of an integrated circuit after a first fabrication stage;

FIG. 2 is a cross-sectional view of the integrated circuit after a second fabrication stage;

FIG. 3 is a cross-sectional view of the integrated circuit after a third fabrication stage;

FIG. 4 is a cross-sectional view of the integrated circuit after a fourth fabrication stage;

FIG. 5 is a top view of the integrated circuit

after the fourth fabrication stage; and

FIG. 6 is a cross-sectional view of the integrated circuit after a fifth fabrication stage.

Detailed Description of the Drawings

[0007] In the figures, elements having the same reference number have similar functionality.

[0008] FIG. 1 is a cross-sectional view of an integrated circuit or semiconductor device 2 formed with a semiconductor substrate 12 after a first processing stage.

[0009] Semiconductor substrate 12 includes a base layer 10 formed to have a thickness of about two hundred and fifty micrometers. In one embodiment, base layer 10 is heavily doped to have a p-type conductivity and a resistivity of about 0.01 ohm-centimeters to function as a ground plane for integrated circuit 2. In one embodiment, base layer 10 comprises monocrystalline silicon.

[0010] An epitaxial layer 30 is grown to a thickness of about three micrometers over base layer 10. In one embodiment, epitaxial layer 30 comprises monocrystalline silicon doped to have a p-type conductivity and a resistivity of about twenty ohm-centimeters.

[0011] A dielectric layer 40 is formed over epitaxial layer 30 to a thickness of about three hundred Angstroms to form a hard mask. In one embodiment, dielectric layer 40 is formed with a thermally grown silicon dioxide.

[0012] A dielectric layer 50 is formed over dielectric layer 40. In one embodiment dielectric layer 50 is formed with plasma enhanced chemical vapor deposition (PECVD) tetra-ethyl-ortho-silicate (TEOS) glass as a blanket silicon dioxide to a thickness of about three thousand Angstroms.

[0013] A surface 13 of substrate 12 is patterned with photoresist to mask a series of standard etch steps that remove exposed portions of dielectric layer 40 and dielectric layer 50. A standard anisotropic silicon etch is then applied to remove exposed portions of epitaxial layer 30 and base layer 10 to concurrently form recessed region or trench 20 within an isolation region 22, and recessed region or trench 21 around an active device region 145'. Isolation region 22 is for forming electrical components such as passive devices and bonding pads, and active region 145 for forming transistors and other active devices.

[0014] Recessed regions 20 and 21 typically are formed concurrently and with the same processing steps. However, in order to accommodate potentially different isolation requirements of active device regions as compared to passive component isolation regions, recessed region 20 within isolation region 22 and recessed region 21 around active device isolation area 145 may have different vertical and lateral dimensions, although processed using the same fabrication steps. In one embodiment, recessed region 20 in is formed to a depth of about five micrometers and a width of about three micrometers. In one embodiment, recessed region 21 is formed to a depth of about five micrometers and a width of about two micrometers.

[0015] FIG. 2 shows a cross-sectional view of integrated circuit 2 after a second fabrication stage. A standard wet chemistry etch is used to clean the recessed region 20, and during this clean TEOS dielectric layer 50 is removed and some of the dielectric layer 40 is removed leaving a portion 45 of dielectric layer 40 as shown.

[0016] In one embodiment, a dielectric layer (not shown) is formed in recessed region 20 over sidewalls 31 of epitaxial layer 30 to a thickness of about three hundred Angstroms to promote adhesion of subsequent layers to the

epitaxial layer.

[0017] A dielectric material 60 is then deposited onto substrate 12 covering the substrate and filling recessed region 20. In one embodiment, dielectric material 60 is silicon dioxide formed with PECVD TEOS deposited at a temperature of about three hundred and fifty degrees centigrade for about thirty minutes. Dielectric material 60 typically has a dielectric constant of about 3.5 and is formed to a thickness of about 4.5 micrometers, filling recessed region 20 above dielectric layer 45.

[0018] Deposited dielectrics such as dielectric material 60 have several advantages over thermally grown films or silicon. For example, thick dielectric films are formed quickly and at low temperatures, have reduced stress, a minimal impact on the overall thermal budget, low cost, and fast etching characteristics. In addition, the dielectric constants typically are lower than many other films or materials used to form low dielectric structures.

[0019] Dielectric material 60 is then subjected to a blanket, timed etch to remove a predetermined thickness, leaving dielectric material within recessed region 20 to a level below dielectric layer 45. In one embodiment, the dielectric material etch back process is performed using reactive ion-etch to a distance 48 below surface 46 to define the thickness of materials deposited in recessed region 20 as described in detail below. In one embodiment, the dielectric material 60 is etched back so that distance 48 is approximately 0.5 micrometers below surface 46.

[0020] A material 70 is deposited onto the substrate 12, covering the surface of substrate 12 and filling trench 20 above dielectric layer 45. In one embodiment, the material 70 is formed with chemical vapor deposition (CVD) polysilicon at a temperature of about six-hundred and twenty five degrees centigrade and a thickness of about four-

thousand five-hundred Angstroms for about forty-five minutes.

[0021] FIG. 3 shows a cross-sectional view of integrated circuit 2 after a third fabrication stage. A standard planarizing etch is performed using dielectric layer 45 as an etch stop. A photo mask layer 80 is applied over the material and used to pattern an etch that removes exposed portions of layer 70 and stops on dielectric material 60 to form a cap layer 75.

[0022] In one embodiment, a compression layer (not shown) comprising CVD silicon nitride at a temperature of about seven hundred eighty degrees centigrade for about eighty minutes to a thickness of about two thousand Angstroms is deposited on top of cap layer 75. When oxidized, this compression layer provides additional lateral expansion of cap layer 75 as a means to seal larger recessed regions during later processing, although for smaller recessed regions this compression layer may not be required.

[0023] FIG. 4 shows a cross-sectional view of integrated circuit 2 after a fourth fabrication stage. Photo mask layer 80 is removed. An etch is performed to remove the dielectric material 60 to a depth 91 of about four and one-half micrometers to form a recessed region or trench 76 that define an array of pillars 65. In one embodiment, the etch is formed using reactive ion etching at a temperature of about three-hundred and fifty degrees centigrade, a pressure of about 250 millitorr, a power of about 1500 watts using the gases sulfur hexafluoride and oxygen until the material is cleared from the bottom 93 of the trench 76.

[0024] A dielectric material 95 is deposited onto walls 92 to provide reinforcement for additional stability under stress and to reduce defects. In one embodiment, dielectric material 95 is formed having a dielectric constant of about 11.8 using CVD polysilicon deposited at a temperature of

about six-hundred and fifty degrees centigrade for about five minutes to a thickness of about five-hundred Angstroms. In another embodiment, dielectric material 95 is formed with amorphous silicon having a dielectric constant of about 11.8 to a thickness of about five-hundred Angstroms using chemical vapor deposition performed at a temperature of about five-hundred fifty degrees centigrade for about twenty-five minutes.

[0025] In an embodiment where recessed region 20 has a small area so stability and defects are less critical, the pillar reinforcement process described above can be left out to reduce costs.

[0026] FIG. 5 is a top view of integrated circuit 2 showing features of isolation region 22 and active region 145 after the processing stage described in FIG. 4. Trench 76 surrounds and effectively defines active region 145 as shown, and within isolation region 22 form a matrix or grid to define pillars 65. As will be apparent from the subsequent processing steps, a variety of alternate arrangements can be used to form the trench 76. For example, an array of holes could be etched to form trench 76, effectively reversing the positions of pillars 65 and trench 76. That is, pillars 65 can be formed as a contiguous matrix while trench 76 are etched as an array of discrete holes. Alternatively, trench 76 may be formed as a series of parallel trenches or recessed regions within isolation region 22. Furthermore, while pillars 65 are shown having a generally rectangular shape, pillars 65 can be of other shapes including generally oval, generally reticulated, and generally elongated.

[0027] FIG. 6 shows a cross-sectional view of integrated circuit 2 after a fifth fabrication stage. Recall that cap

layer 75 is formed with polysilicon, which now is thermally oxidized at a temperature of about one thousand degrees centigrade to form a dielectric material 100 that seals openings of trench 76 to form voids 200. In one embodiment, dielectric material 100 is formed with a dielectric constant of about 3.8 to a thickness of approximately 0.2 micrometers above EPI layer 30. Depending on the dimensions of the trench 76, some of the silicon material 175 of cap layer 75 may not be converted to silicon dioxide. For example, if the dimensions are suitable and a shorter oxidation step is desired, complete oxidation of cap layer 75 is not needed to seal recessed region 76. Note that by thermally oxidizing cap layer 75 to produce the dielectric material 100 sealing the openings of the trench 76, the invention avoids the problem of prior art in which void sealing material is also substantially deposited into the trench resulting in voids with less gaseous volume, thus higher dielectric constant.

[0028] Dielectric material 100 is patterned and/or removed in the active region and an active device 140 such as an n-channel metal-oxide-semiconductor field-effect transistor is formed as follows. A dielectric material is thermally grown over epitaxial layer 30 and a polysilicon material is deposited over the dielectric material. The polysilicon and dielectric materials are patterned and etched to form a gate dielectric 143 and an overlying gate electrode 144 of transistor 140 as shown. Gate dielectric 143 and gate electrode 144 are used in combination with a photoresist layer (not shown) to form a mask for introducing n-type dopants into epitaxial layer 30 to form a self-aligned source 141 and drain 142 of transistor 140. In one embodiment, source 141 and drain 142 are heavily doped and formed to a depth of about one-half micrometer.

[0029] The region between the pillars 90 that have been sealed off to produce voids 200 are so designated because they are filled with a gaseous material, which in one embodiment may be air. Voids 200 may also be filled with argon or another ambient gas that is present when the trench 76 become sealed off.

[0030] Note that voids 200 are formed early in the process, i.e., before transistor 140 is formed. For some processes required to form transistor 140 it may be advantageous to leave the step of sealing as described above until the gate dielectric 143 formation such that any concerns of gases trapped in the voids are eliminated, or to accommodate the transistor thermal processing budget. The simple process described above is compatible with standard semiconductor processing, has a low thermal budget, and can be implemented at virtually any point of an active device fabrication process.

[0031] Dielectric material is deposited on substrate 12 and planarized to re-form the layer 100 as shown in FIG.6. Dielectric material 100 may also function as an interlayer dielectric that separates metallization interconnect layers.

[0032] The effective dielectric constant of isolation region 22 is a combination of the dielectric constant or permittivity of voids 200 and the permittivity of the material used to form the pillars 65, and dielectric material 100. In one embodiment, the gaseous material contained in voids 200 has a dielectric constant substantially equal to one, and the wall reinforcement material 95 has a dielectric constant of about 3.8, thus the overall dielectric constant of the isolation region formed is less than 3.8, depending on the relative volumes of pillars 65, reinforcement material 95, and voids 200. Thus, the invention avoids the problem of prior art in which the isolation region 22 is comprised of gas, dielectric

material, and semiconductor material thus producing a isolation region having a correspondingly higher dielectric constant. Hence, isolation region 22 has a low effective permittivity for forming electrical components with a low parasitic substrate capacitance.

[0033] An electrical component 120 is formed on dielectric material 100 over isolation region 22. Electrical component 120 has a low parasitic capacitance to substrate 12, and therefore a higher frequency capability, because of the low permittivity of isolation region 22. Electrical component 120 may be a bonding pad, a passive component such as an inductor, capacitor or resistor, or another electrical device suitable for formation over a dielectric material.

[0032] In summary, the present invention provides a semiconductor device comprising a semiconductor substrate having a surface formed with a first recessed region; a first dielectric material deposited in the first recessed region and formed with a second recessed region; and a second dielectric material grown over the first dielectric material to seal the second recessed region.